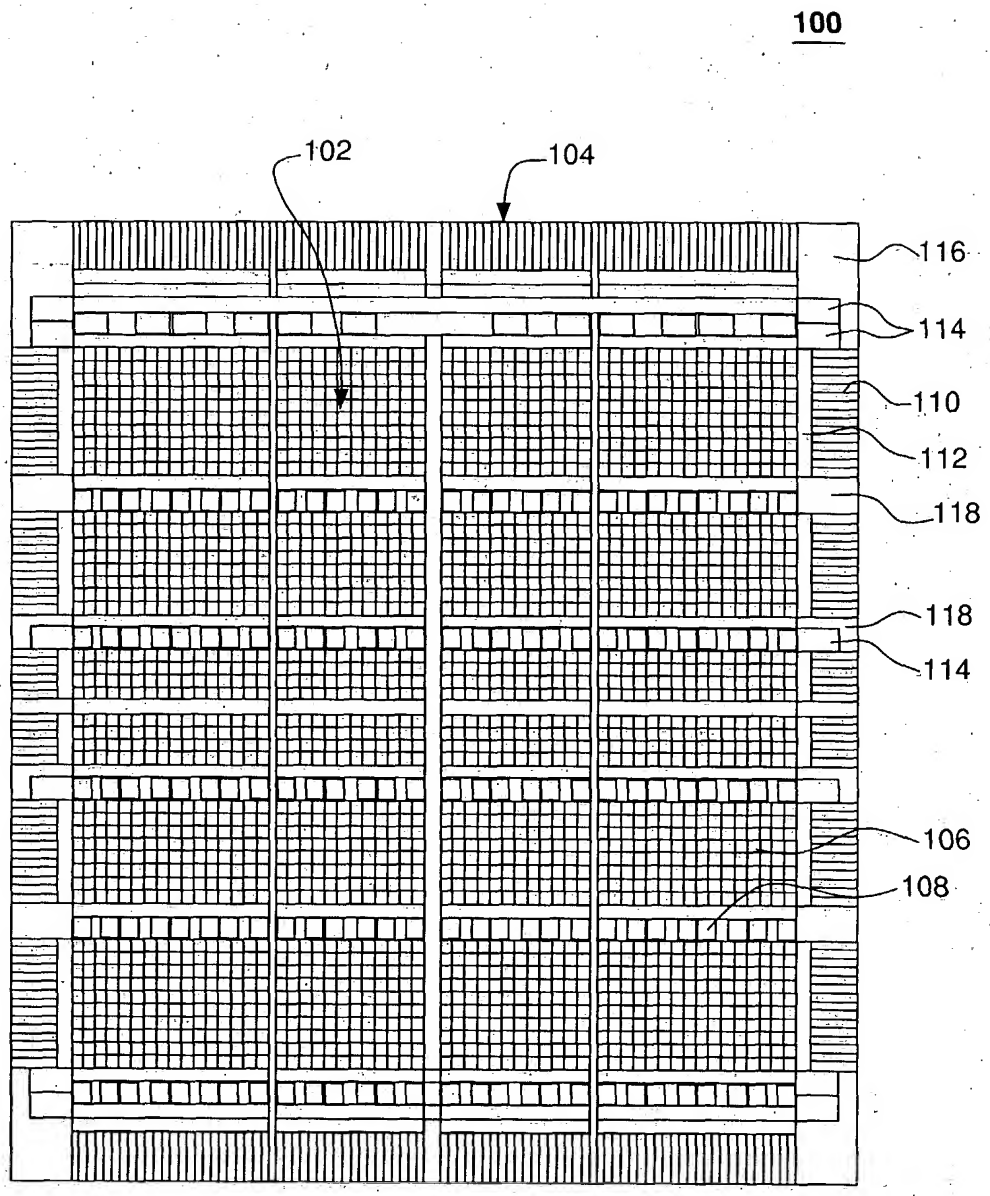

FIG. 1

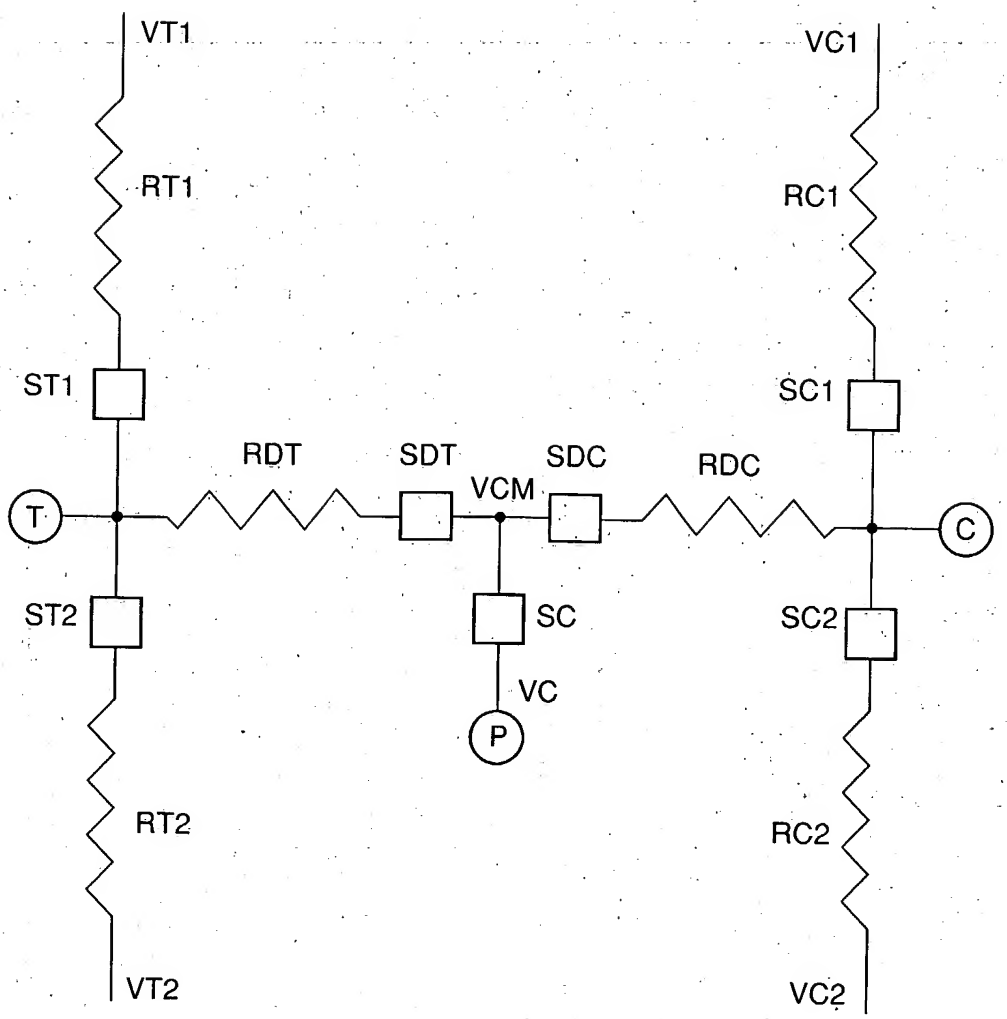
VT1
RT1
ST1
RDT
SDT
VCM
SDC
RDC
VC1
RC1
SC1
T
C
ST2
SC
VC
P
SC2
RT2
RC2
VT2
VC2

FIG. 2

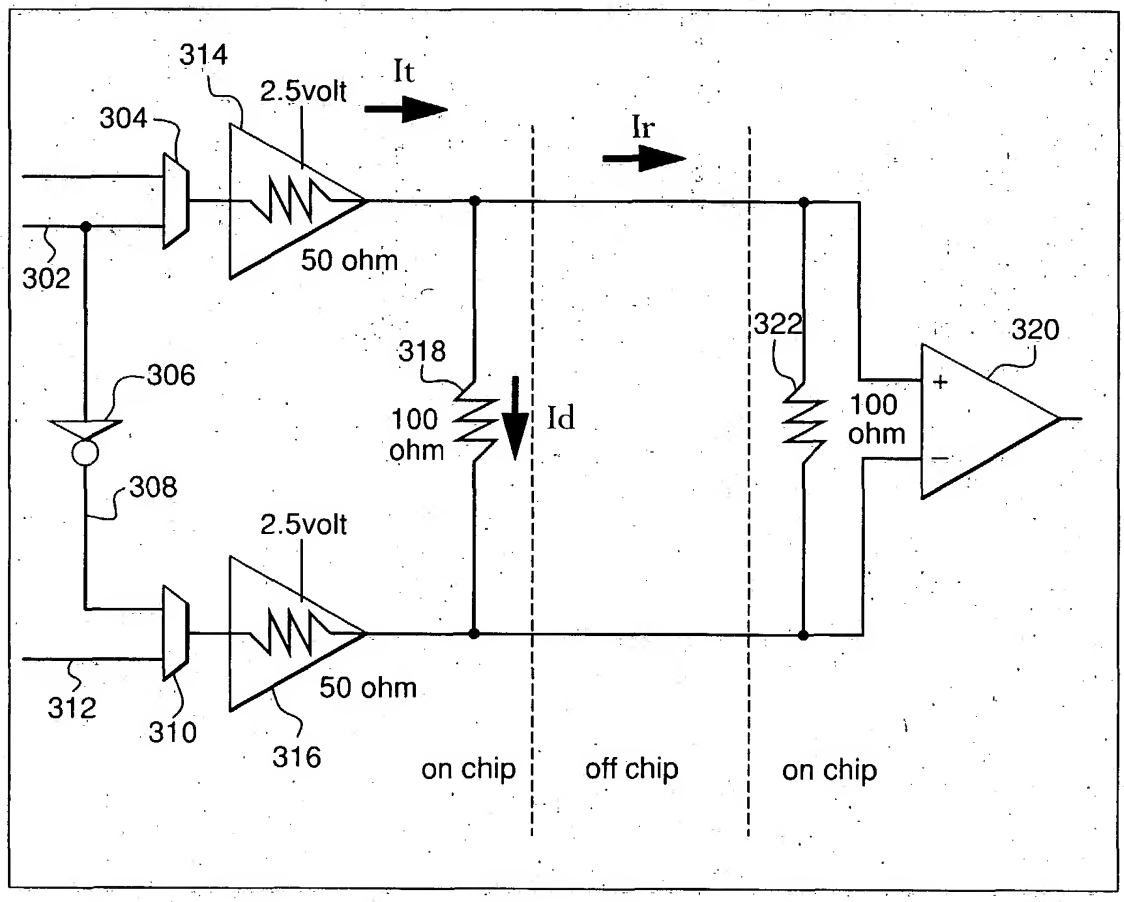
314
2.5volt
It
304
Ir
302
50 ohm
322
320
318
306
100
ohm
Id
100
ohm
308
2.5volt
50 ohm
312
310
316
on chip
off chip
on chip

FIG. 3

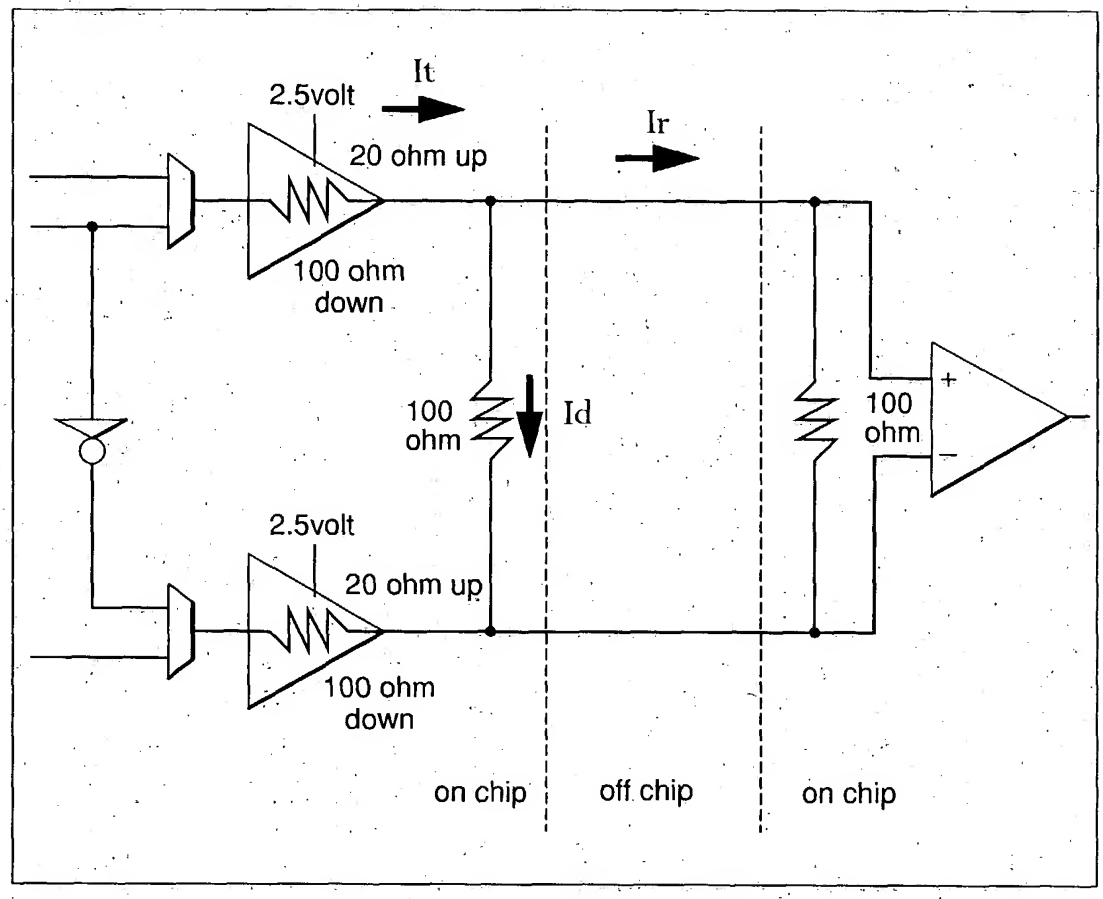
It
2.5volt
20 ohm up
Ir
100 ohm
down
100
ohm
Id
100
ohm
+
−
2.5volt
20 ohm up
100 ohm
down
on chip
off chip
on chip

FIG. 4

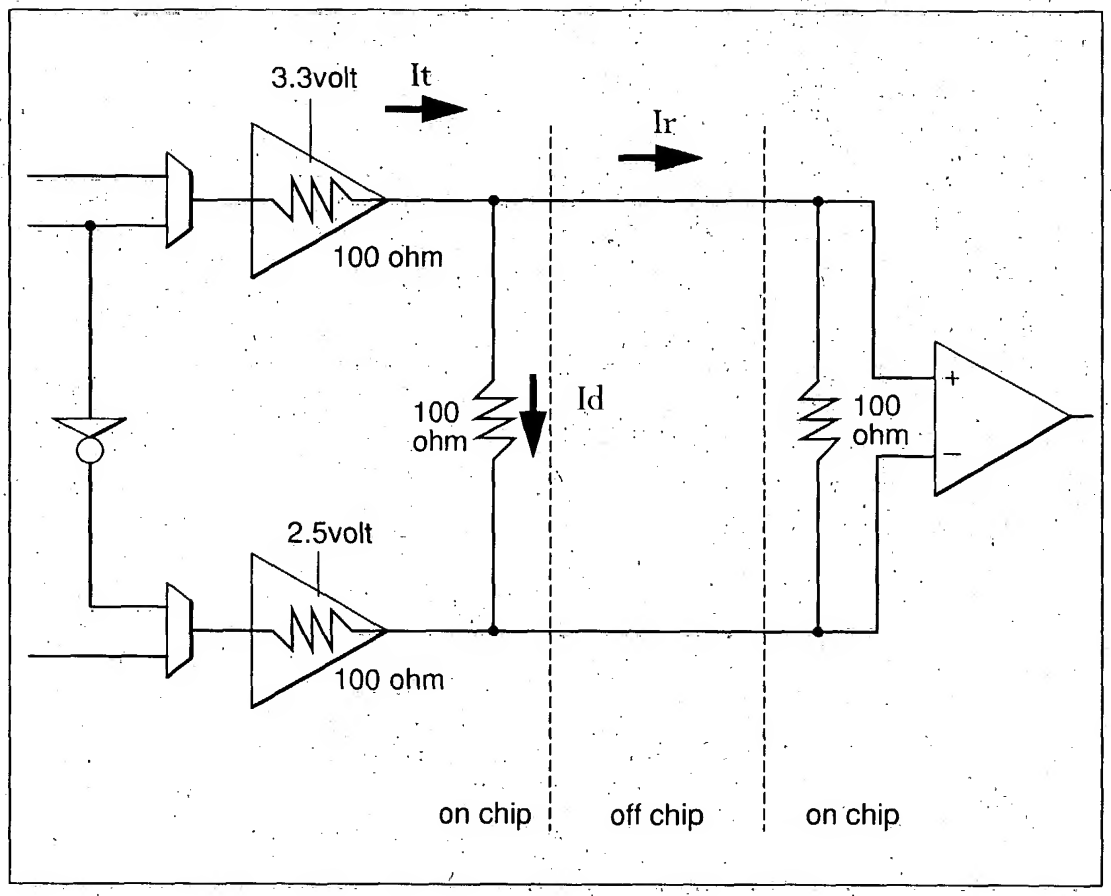
3.3volt
It
Ir
100 ohm
100
ohm
Id
100
ohm
+
–
2.5volt
100 ohm
on chip
off chip
on chip

FIG. 5

Table I : Summary using on-chip termination schemes

	Fig. 3	Fig. 4	Fig. 5	External Impedance option	LVPECL SPEC
VDDIO	2.5v	2.5v	3.3v	3.3v	
output impedance up	50 ohm	20 ohm	100 ohm	100 ohm	
output impedance down	50 ohm	100 ohm	100 ohm	100 ohm	
Differential Impedance	Internal 100 ohm	Internal 100 ohm	Internal 100 ohm	External 200 ohm	
It	16.7mA	14.7mA	13.2mA	12.4mA	
Ir	8.35mA	7.35mA	6.6mA	4.1mA	
Id	8.35mA	7.35mA	6.6mA	8.3mA	
Voh	1.670v	2.206v	1.980v	2.06v	1.975v - 2.720v
Vol	0.835v	1.470v	1.320v	1.24v	1.190v - 1.980v
Vod	0.835v	0.740v	0.660v	0.830v	0.600v - 1.000v
Vcm	1.250v	1.838v	1.650v	1.65v	1.582v - 2.350v
driver power VDDIO*It	41.8mW	36.8mW	43.6mW	40.9mW	

FIG. 6

TABLE II			
ELEMENT	Fig. 3	Fig. 4	Fig. 5
RT1	50 ohms	20 ohms	100 ohms
RT2	50 ohms	100 ohms	100 ohms
RC1	50 ohms	20 ohms	100 ohms
RC2	50 ohms	100 ohms	100 ohms
RDT	50 ohms	50 ohms	50 ohms
RDC	50 ohms	50 ohms	50 ohms
VT1	2.5V	2.5V	3.3V
VC1	2.5V	2.5V	3.3V
VT2	0V	0V	0V
VC2	0V	0V	0V

FIG. 7

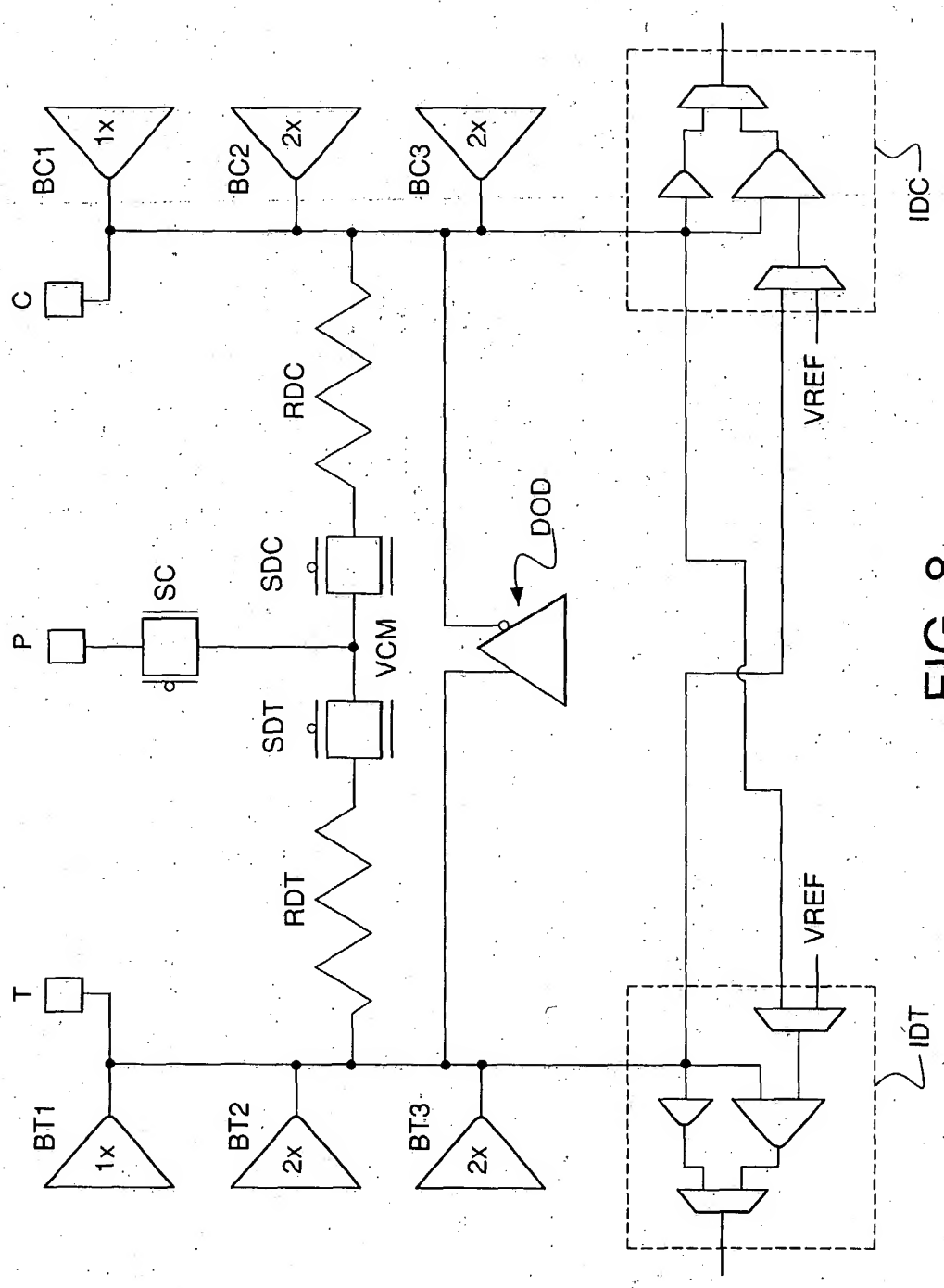
800
BC1
1x
BC2
2x
BC3
2x
C
RDC
SDC
SC
P
VCM
SDT
RDT
DOD
T
BT1
1x
BT2
2x
BT3
2x
VREF
IDC
VREF
IDT

FIG. 8

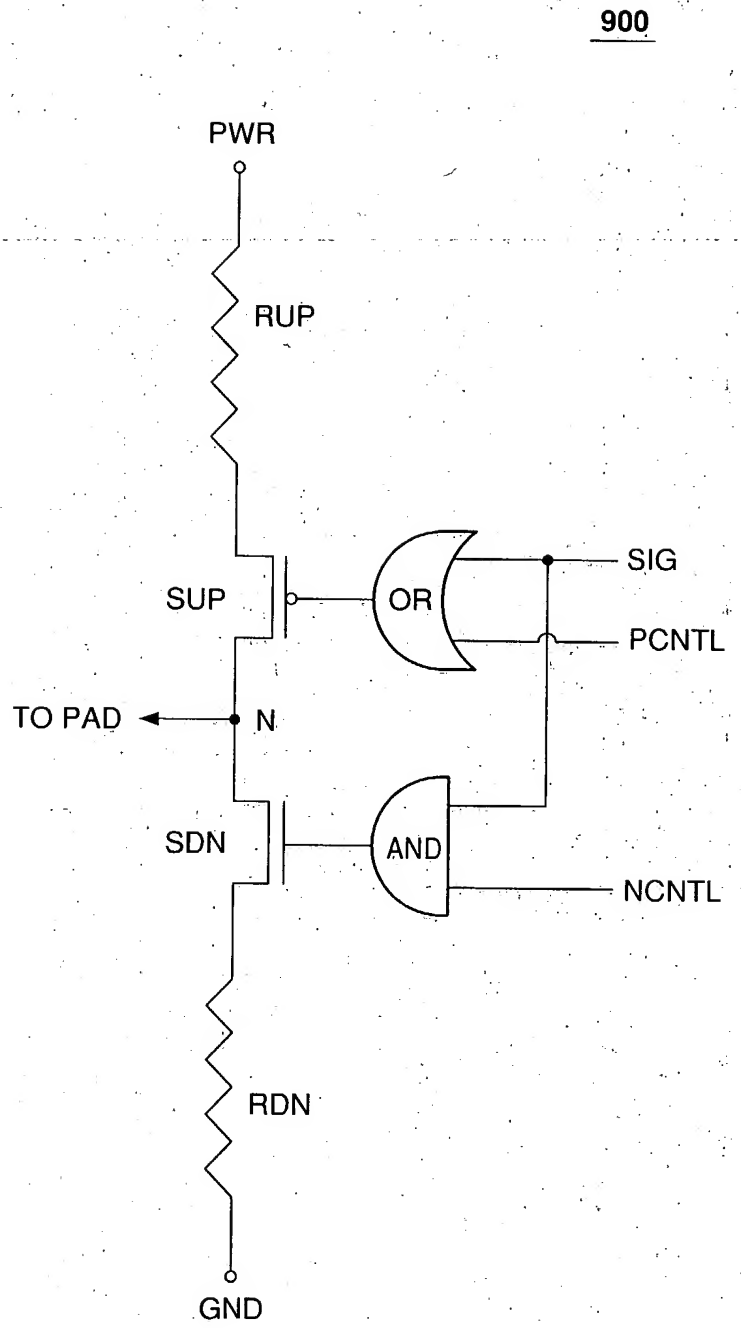

FIG. 9